



A Rule-based Method for Minimizing Power Dissipation by Reducing Switching Activity of Digital Circuits

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A Rule-based Method for Minimizing Power Dissipation by Reducing Switching Activity of Digital Circuits

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A s r c — Minimization of power dissipation of VLSI circuits is one of the major concerns of recent digital circuit design primarily due to the ever decreasing feature sizes of circuits, higher clock frequencies and larger die sizes. The primary contributors to power dissipation in digital circuits include leakage power; short-circuit power, and switching power. Of these, power dissipation due to circuit switching activity constitutes the major component. As such, an effective mechanism to minimize power loss in such cases often involves the minimization of switching activity. In this paper, we propose an intelligent rule-based algorithm for reducing the switching activity of digital circuits at logic optimization stage. The proposed algorithm is empirically tested for several standard digital circuits with Synopsis EDA tool and results obtained are quite encouraging.

ey ords — Switching Activity, low-power VLSI circuits, CMOS, Power dissipation, dynamic power, electromigration.

1 INTRODUCTION

Traditionally, the major concerns of the VLSI designers include minimization of chip area, enhancement of performance, testability, reduction of manufacturing cost and improvement of reliability. With increasing use of portable devices and wireless communication systems, reduction of energy consumption and hence reduction of power dissipation and optimization of chip temperature have become some recent major concerns in VLSI design [17]. Power dissipated by a digital system increases the temperature of the chip and affects battery life of the digital devices [14]. Aggressive device scaling also causes excessive increase in power per unit area of the chip. This high power dissipation in VLSI devices is usually manifested in the form of rise of chip temperature. As such, heat generation and its removal from a chip are of serious concern [2]. The heat removal system must be efficient and must keep the junctions below a certain threshold, as determined by reliability constraints. With higher level of integration more and more transistors are being packed into smaller areas. Thus, for high level of integration, heat removal is a dominant design factor. In absence of appropriate removal of the generated heat, the chip temperature may rise causing thermal breakdown. One of the major reasons of VLSI chip failure is due to interconnect failure, often attributed to the phenomenon of electromigration, causing leakage power. The mean time to failure (MTTF) of interconnect due to electromigration is given by Black's equation [7]

$$MTTF = A_j^{-2} e^{\left(\frac{Q}{KT}\right)} \quad (1)$$

where A is a constant based on the given

resistance of the transistors consumes electrical e

is presented in [8] using the general delay model. An analytical approach to compute the switching activity of digital circuits at word-level in the presence of glitches and correlation is presented in [16]. The work in [5] provides an interesting repository of recent techniques of power modeling and low power design based on high-level synthesis. The evaluation and reduction of switching activity in combinational logic circuits considering both the transitions $1 \rightarrow 0$ and $0 \rightarrow 1$ at any output node is proposed in [15]. In order to satisfy the classical probabilistic approach that limits the maximum value of switching activity to 1 the definition of switching activity as proposed in [15] was customized in [19]. An algorithmic approach at the Gate level using k-map

$$P_1 = \frac{|N_i|}{|N_i| + |X_i|} \quad (4)$$

Def n on For a given node of a circuit the probability of transition either from 0 to 1 or from 1 to 0 is known as switching activity (SA) of that node.

Thus, switching activity of node i is given by the composite probability

$$SA = P_0 + P_1 = \frac{|N_i| + |X_i|}{[|N_i| + |X_i|]^2} \quad (5)$$

For instance the switching activity of 2-input AND Gate ($|N_i| = 1$ and $|X_i| = 3$) is given by $\frac{3}{16}$ and this contributes to the dynamic power loss of the AND Gate.

As already mentioned, power dissipation in digital circuits can be reduced by minimizing its total switching activity. In order to minimize the switching activity one must know the minimum and maximum values of switching activity for the logical expression for a particular switching circuit. The total numbers of values (0's and 1's) in the output column of a truth table are dependent solely on the number of inputs and thus may be considered to be invariant for a given

Consider a logical expression $f = \bar{a}\bar{b}c + \bar{a}b\bar{c} + \bar{a}bc + \bar{a}bcd$. The switching activity for $f_1 = \bar{a}\bar{b}c$ is $\frac{7}{64}$. This is due to the fact that the output is 1 only for the input vector 101. As such, the number of 1's and 0's in the output column are respectively 1 and 7. For the implementation of $f_1 = \bar{a}\bar{b}c$, a NOT Gate is required for \bar{b} , having switching activity $\frac{1}{4}$, an AND gate is required for ac with switching activity $\frac{3}{16}$. The outputs of these NOT Gate and AND Gate are inputs to a second AND Gate having switching activity $= \frac{7}{64}$. The total switching activity for f_1 is thus $\frac{1}{4} + \frac{3}{16} + \frac{7}{64}$.

Clearly, the switching activities for both $f_2 = ab$ and $f_3 = \bar{c} + d$ are $\frac{3}{16}$. When represented as a minterm, the function is given by $f = \sum_{i=0,1,2,3,4,5,6,7,8,9,10,11,12} m_i$ and the activity is $\frac{39}{256}$ (as $|N_i|=3, |X_i|=13$). Thus, the total switching activity of the circuit is $\frac{1}{4} + \frac{3}{16} + \frac{7}{64} + \frac{7}{64} + \frac{3}{16} + \frac{3}{16} + \frac{39}{256} = \frac{303}{256}$ (Figure 1).

4 MOTIVATION OF THE WORK

According to International Technology Roadmap for Semiconductor (ITRS) one of the major goals of the semiconductor industry is to be able to continue to scale the technology in overall performance. The performance of the components and the final chip can be measured in many

logical expression of the switching functions. Logic optimization is often achieved using the standard SOP or POS expression. However, the focus of earlier works in logic optimization is primarily on the reduction of number of input terms or number of literals [6]. An algorithm for interconnection-aware two-level logic optimization of multi-output SOP functions appears in

Observation If a sum-of-product expression contains pair-wise common Boolean literals with multiplication distributed over addition like $f1 = A.B + B.C$ then modification of this expression applying converse distributive property i.e. $f1 = A.B + B.C \Rightarrow f2 = B.(A + C)$ reduces the number of gates as well as switching activity. Figure 5 shows the reduction of switching activity due to 6224.67 m (s)

2-variable Boolean expressions according to Lemma 2. This Lemma 2 can be effectively used to reduce the switching activity if the number of complemented term is odd. Hence this Lemma 2 can be applied in the proposed method described in this paper if $n \geq 2$ and n is even.

Le : For an

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For $n=2$, $t_2 = \frac{1}{2^2} + \frac{1}{2^4} + \frac{1}{4} + \frac{1}{64} + \frac{3}{16} + \frac{1}{4}$. Let us assume that the results holds for $n=k$ variables. i.e. $t_k = \frac{1}{2^k} + \frac{1}{2^{2k}} + \frac{1}{4}$. Now we need to show that the result also holds for $n = k + 1$ variables. $t_{(k+1)} = \frac{1}{2^{(k+1)}} + \frac{1}{2^{2(k+1)}} + \frac{1}{2} \left[\frac{1}{2^k} + \frac{1}{2^{2k}} \right] + \frac{1}{2^{(2k+1)}} + \frac{1}{2} t_k + \frac{1}{2^{(2k+1)}} + \frac{1}{4}$ □

Le If a product term in a logical expression contains odd number of complemented literals, then switching activity can be reduced by replacing pair of complemented literals with their NOR combination and replacing remaining one complemented literal $\overline{x_i}$ by $x_i - 1$. And if product term contains only one complemented literal $\overline{x_i}$ then switching activity can be reduced by replacing complemented literal $\overline{x_i}$ by $x_i - 1$.

Proof [By Induction]

We consider a product term in a logical expression containing two literals of the form $x\overline{y}$. From Figure 17a and Figure 17c it is evident that the switching activity for \overline{y} is $\frac{1}{4}$ and that of for $x\overline{y}$ is $\frac{3}{16}$. Thus, the total switching activity in this case is given by

$$TSA_{21c} = \frac{1}{4} + \frac{3}{16} = \frac{7}{16} \quad (8)$$

(TSA_{ijc} represents Total Switching Activity of a product term containing i number of literals out of which j number of literals are in complemented form and TSA_{ijm} represents the same of a modified product term.)

Now the expression $x\overline{y}$ can be modified as $x(y - 1) = xy - x$. Corresponding truth table and circuit diagram are shown in Figure 17c and Figure 17b respectively.

From Figure 17c and Figure 17b the switching activity for xy is $\frac{3}{16}$ and that of for $xy - x$ is $\frac{3}{16}$. So total switching activity in this case

$$TSA_{21m} = \frac{3}{16} + \frac{3}{16} = \frac{6}{16} \quad (9)$$

Thus, from the equations 12 and 13 it is clear that $TSA_3 3m = TSA_3 3c$. Thus, product terms containing 2 and 3 literals with odd number of comp

Proof This Lemma is basically the generalized form of Lemma 10 as

$$- \quad - \quad p \quad \text{-----} \quad \frac{\text{-----}}{k} \quad \frac{\text{-----}}{k} \quad \frac{\text{-----}}{l} \quad \frac{\text{-----}}{l}$$

Algorithm Minimize Switching Activity ()

Input: Truth Table

Output: Function for minimal switching activity

1. Obtain the minimal Sum-of-Product (f_{SOP}) or Product-of-Sum (f_{POS}) expression using any standard method for the minimization of given switching function f .
2. Apply Rule 1 and Rule 2 to reduce the switching activity
3. If either the (f_{SOP}) or (f_{POS}) does not contain any complemented variable then
Calculate the total switching activity of the function corresponding to (f_{SOP}) or (f_{POS}).
4. Take the function with minimum switching activity.
5. Endif
6. If the product term in f_{SOP} contains even number of complemented terms then
7. Replace a pair of complemented terms by their corresponding NOR combination using De' Morgan's theorem (Rule 3).
8. Endif
9. If the sum term in f_{POS} contains even number of complemented terms then
10. Replace a pair of complemented terms by NAND Gate using De, Morgan's theorem (Rule 3).
11. Endif
12. If applicable then
13. Apply Rule 4, Rule 6, Rule 7, Rule 9, Rule 10, and Rule 11 to reduce the switching activity.
14. Endif
15. If a f_{SOP} (f_{POS}) contains only one complemented term x_i then
16. Apply Rule 8 or Rule 12 (in case of SOP) from Iy-26 Tm994()JTJ -257.553 -20.64 7d [(1)-3.58076(6)

8 EXPERIMENTAL RESULTS

The proposed rule-based algorithm is implemented in Xilinx 14.7 and power estimation has been done using Synopsys EDA tool -DESIGN VISION version I-2013.12-SP1, 20, 2014 under CENT OS and using TSMC 120 nm library.

Without loss of generality, for our simulations, we consider only 2-input logic gates. The switching activity of some basic circuits and the associated dynamic power dissipation using conventional SOP (POS) method and our proposed method are summarized in Table 4.

We observe that the total number of switching activity for our proposed method never exceeds, and is less in most of the cases than those obtained using the traditional logic optimization.

Comparison of our proposed method with the existing method of [20]

Reduction of switching activity and hence power dissipation of VLSI CMOS circuits by our proposed algorithm is applicable for any number of input variables and any kind of circuits. In [20] the authors basically modify the k-map to reduce the switching activity. Logic optimization using k-map is limited to 6 variables. Moreover, th

designed using rule-based algorithm proposed in this paper is interestingly applicable for any number of variables. Experimental results show over 34% reduction of switching activity. The works presented in this paper can be further improved by considering both delay and power as objective functions.

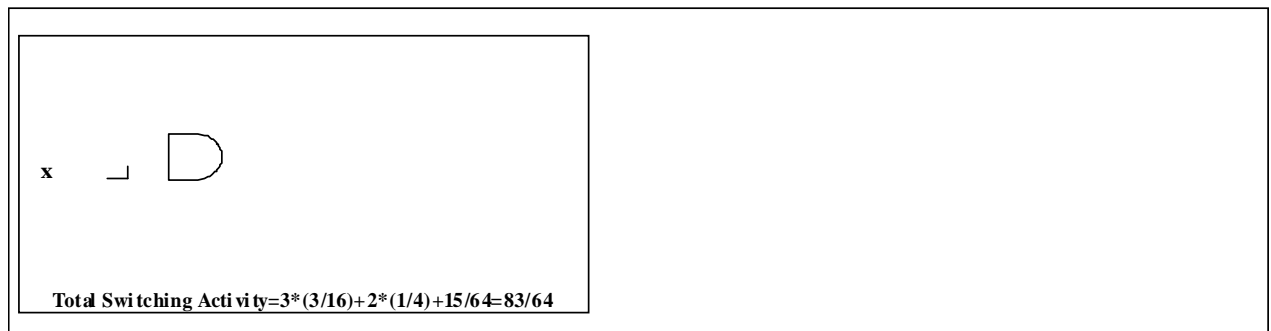
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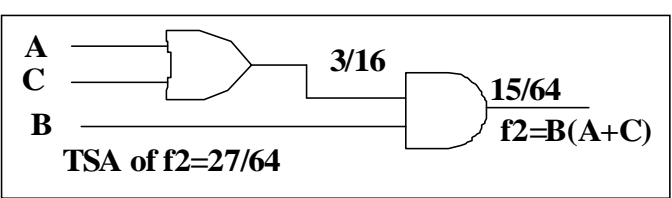
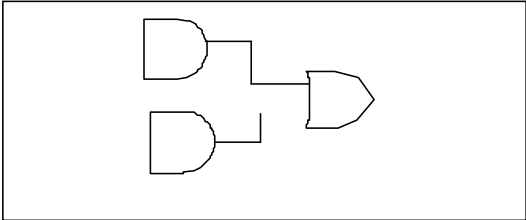
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100-111-121-131-141-151-161-171-181-191-201-211-221-231-241-251-261-271-281-291-301-311-321-331-341-351-361-371-381-391-401-411-421-431-441-451-461-471-481-491-501-511-521-531-541-551-561-571-581-591-601-611-621-631-641-651-661-671-681-691-701-711-721-731-741-751-761-771-781-791-801-811-821-831-841-851-861-871-881-891-901-911-921-931-941-951-961-971-981-991-1001-1011-1021-1031-1041-1051-1061-1071-1081-1091-1101-1111-1121-1131-1141-1151-1161-1171-1181-1191-1201-1211-1221-1231-1241-1251-1261-1271-1281-1291-1301-1311-1321-1331-1341-1351-1361-1371-1381-1391-1401-1411-1421-1431-1441-1451-1461-1471-1481-1491-1501-1511-1521-1531-1541-1551-1561-1571-1581-1591-1601-1611-1621-1631-1641-1651-1661-1671-1681-1691-1701-1711-1721-1731-1741-1751-1761-1771-1781-1791-1801-1811-1821-1831-1841-1851-1861-1871-1881-1891-1901-1911-1921-1931-1941-1951-1961-1971-1981-1991-2001-2011-2021-2031-2041-2051-2061-2071-2081-2091-2101-2111-2121-2131-2141-2151-2161-2171-2181-2191-2201-2211-2221-2231-2241-2251-2261-2271-2281-2291-2301-2311-2321-2331-2341-2351-2361-2371-2381-2391-2401-2411-2421-2431-2441-2451-2461-2471-2481-2491-2501-2511-2521-2531-2541-2551-2561-2571-2581-2591-2601-2611-2621-2631-2641-2651-2661-2671-2681-2691-2701-2711-2721-2731-2741-2751-2761-2771-2781-2791-2801-2811-2821-2831-2841-2851-2861-2871-2881-2891-2901-2911-2921-2931-2941-2951-2961-2971-2981-2991-3001-3011-3021-3031-3041-3051-3061-3071-3081-3091-3101-3111-3121-3131-3141-3151-3161-3171-3181-3191-3201-3211-3221-3231-3241-3251-3261-3271-3281-3291-3301-3311-3321-3331-3341-3351-3361-3371-3381-3391-3401-3411-3421-3431-3441-3451-3461-3471-3481-3491-3501-3511-3521-3531-3541-3551-3561-3571-3581-3591-3601-3611-3621-3631-3641-3651-3661-3671-3681-3691-3701-3711-3721-3731-3741-3751-3761-3771-3781-3791-3801-3811-3821-3831-3841-3851-3861-3871-3881-3891-3901-3911-3921-3931-3941-3951-3961-3971-3981-3991-4001-4011-4021-4031-4041-4051-4061-4071-4081-4091-4101-4111-4121-4131-4141-4151-4161-4171-4181-4191-4201-4211-4221-4231-4241-4251-4261-4271-4281-4291-4301-4311-4321-4331-4341-4351-4361-4371-4381-4391-4401-4411-4421-4431-4441-4451-4461-4471-4481-4491-4501-4511-4521-4531-4541-4551-4561-4571-4581-4591-4601-4611-4621-4631-4641-4651-4661-4671-4681-4691-4701-4711-4721-4731-4741-4751-4761-4771-4781-4791-4801-4811-4821-4831-4841-4851-4861-4871-4881-4891-4901-4911-4921-4931-4941-4951-4961-4971-4981-4991-5001-5011-5021-5031-5041-5051-5061-5071-5081-5091-5101-5111-5121-5131-5141-5151-5161-5171-5181-5191-5201-5211-5221-5231-5241-5251-5261-5271-5281-5291-5301-5311-5321-5331-5341-5351-5361-5371-5381-5391-5401-5411-5421-5431-5441-5451-5461-5471-5481-5491-5501-5511-5521-5531-5541-5551-5561-5571-5581-5591-5601-5611-5621-5631-5641-5651-5661-5671-5681-5691-5701-5711-5721-5731-5741-5751-5761-5771-5781-5791-5801-5811-5821-5831-5841-5851-5861-5871-5881-5891-5901-5911-5921-5931-5941-5951-5961-5971-5981-5991-6001-6011-6021-6031-6041-6051-6061-6071-6081-6091-6101-6111-6121-6131-6141-6151-6161-6171-6181-6191-6201-6211-6221-6231-6241-6251-6261-6271-6281-6291-6301-6311-6321-6331-6341-6351-6361-6371-6381-6391-6401-6411-6421-6431-6441-6451-6461-6471-6481-6491-6501-6511-6521-6531-6541-6551-6561-6571-6581-6591-6601-6611-6621-6631-6641-6651-6661-6671-6681-6691-6701-6711-6721-6731-6741-6751-6761-6771-6781-6791-6801-6811-6821-6831-6841-6851-6861-6871-6881-6891-6901-6911-6921-6931-6941-6951-6961-6971-6981-6991-7001-7011-7021-7031-7041-7051-7061-7071-7081-7091-7101-7111-7121-7131-7141-7151-7161-7171-7181-7191-7201-7211-7221-7231-7241-7251-7261-7271-7281-7291-7301-7311-7321-7331-7341-7351-7361-7371-7381-7391-7401-7411-7421-7431-7441-7451-7461-7471-7481-7491-7501-7511-7521-7531-7541-7551-7561-7571-7581-7591-7601-7611-7621-7631-7641-7651-7661-7671-7681-7691-7701-7711-7721-7731-7741-7751-7761-7771-7781-7791-7801-7811-7821-7831-7841-7851-7861-7871-7881-7891-7901-7911-7921-7931-7941-7951-7961-7971-7981-7991-8001-8011-8021-8031-8041-8051-8061-8071-8081-8091-8101-8111-8121-8131-8141-8151-8161-8171-8181-8191-8201-8211-8221-8231-8241-8251-8261-8271-8281-8291-8301-8311-8321-8331-8341-8351-8361-8371-8381-8391-8401-8411-8421-8431-8441-8451-8461-8471-8481-8491-8501-8511-8521-8531-8541-8551-8561-8571-8581-8591-8601-8611-8621-8631-8641-8651-8661-8671-8681-8691-8701-8711-8721-8731-8741-8751-8761-8771-8781-8791-8801-8811-8821-8831-8841-8851-8861-8871-8881-8891-8901-8911-8921-8931-8941-8951-8961-8971-8981-8991-9001-9011-9021-9031-9041-9051-9061-9071-9081-9091-9101-9111-9121-9131-9141-9151-9161-9171-9181-9191-9201-9211-9221-9231-9241-9251-9261-9271-9281-9291-9301-9311-9321-9331-9341-9351-9361-9371-9381-9391-9401-9411-9421-9431-9441-9451-9461-9471-9481-9491-9501-9511-9521-9531-9541-9551-9561-9571-9581-9591-9601-9611-9621-9631-9641-9651-9661-9671-9681-9691-9701-9711-9721-9731-9741-9751-9761-9771-9781-9791-9801-9811-9821-9831-9841-9851-9861-9871-9881-9891-9901-9911-9921-9931-9941-9951-9961-9971-9981-9991-10001-10011-10021-10031-10041-10051-10061-10071-10081-10091-10101-10111-10121-10131-10141-10151-10161-10171-10181-10191-10201-10211-10221-10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Figures and Tables

Figure1. Switching Activity for $\overline{abc} + \overline{ab} + \overline{c} + d$





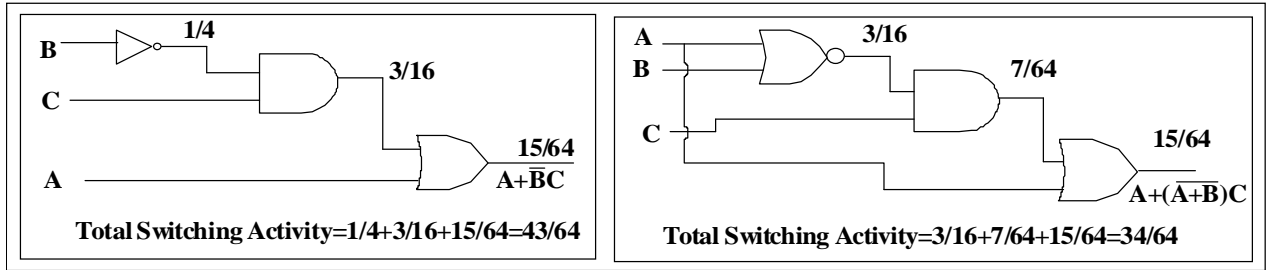
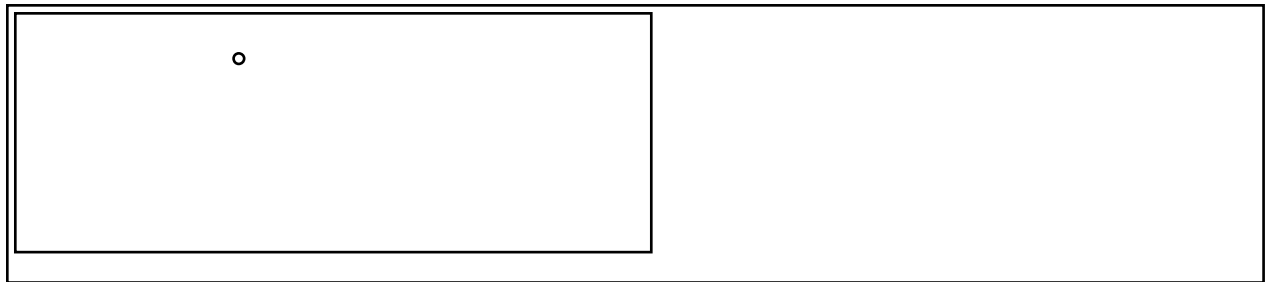
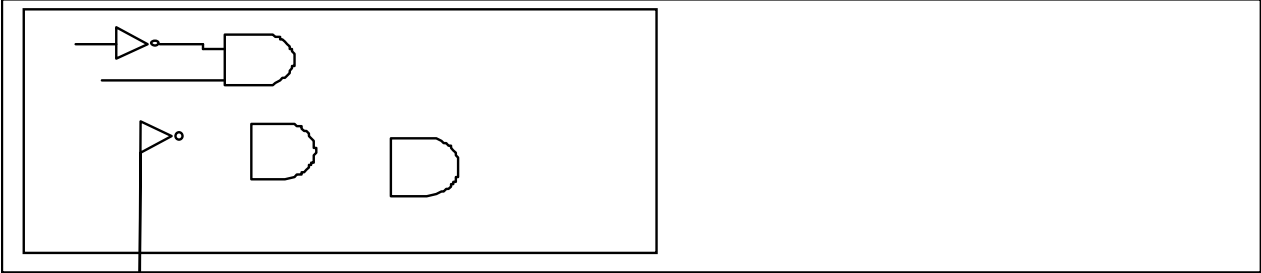
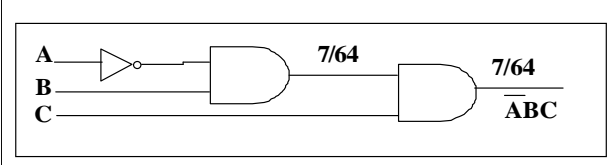


Figure 9: Switching Activity for $A + \overline{B}C$ and $A + (\overline{A+B})C$







(4)

A	B	\overline{A}	$\overline{A+B}$	AB	$\overline{A+AB}$	$\overline{A+B+B}$
0	0	1	1	0	1	1
0	1	1	0	0	1	1
1	0	0	0	0	0	0
1	1	0	0	1	1	1

Table 2: Truth table for $\overline{A+AB}$ and $\overline{A+B+B}$

z y x
 0 0 0 1 1